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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,438	KAO ET AL.	
	Examiner	Art Unit	
	Elias Ullah	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 4/9/04 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application and IDS filed 4/09/2004.

2. The information disclosure statement (IDS) submitted on 4/9/2004 is being considered by the examiner.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-15, drawn to method of forming an integrated circuit transistor, classified in class 438, subclass 305+.

   II. Claims 16-22, drawn to integrated circuit device, classified in class 257, subclass 387.

The inventions are distinct, each from the other because of the following reasons:

4. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process, i.e a process which does not require to form a dielectric layer overlaying the semiconductor substrate first and the first doped region. Instead, the doped region can be formed and then the dielectric layer.

5. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Mr. McClure on 1/17/206 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-22 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Objections

8. Claims 1 and 10 are objected to because of the following informalities: On page 20, line 23 and page 24, line 3, "proving" should be spell providing. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-8, 10 and 12-15 rejected under 35 U.S.C. 102(e) as being anticipated by anticipated by Baw-Ching Perng et al. (6,498,067 dated 12/24/2002).

11. With respect to claim 1, Baw-Ching Perng et al. shows the method as claimed in figures 1-7 as: a method of forming an integrated circuit transistor, comprising: proving a semiconductor substrate with gate structure formed thereon (Fig. 1, 1, 3); forming at least one dielectric layer(5) overlying the semiconductor substrate (1), wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure along the surface of the semiconductor substrate; forming at least one first doped region (4) in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer (4), wherein the at least one second portion of the at least one dielectric layer remains overlying the at least one first doped region (4) ; forming a sidewall spacer (6b) overlying the at least one dielectric layer along the at least one sidewall of the gate structure; and forming at least one second doped region (7) in the semiconductor substrate laterally adjacent to the sidewall spacer.

12. With respect to claim 2, Baw-Ching Perng et al. also shows the method as claimed as: a thickness of the at least one dielectric layer ranges from about 10 angstroms to about 350 Angstroms (Col. 3, lines 51-53).

13. With respect to claim 3, Baw-Ching Perng et al. also shows the method as claimed as: a step of removing exposed regions of the at least one dielectric layer before the formation of the at least one second doped region (Fig. 6, col. 5, lines 5-10).

14. With respect to claim 4, Baw-Ching Perng et al. also shows the method as claimed as: the formation of the at least one dielectric layer is a blanket deposition of silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof (col.3, lines 51-55).

15. With respect to claim 6, Baw-Ching Perng et al. also shows the method as claimed as: the sidewall spacer is silicon oxide, silicon oxynitride, alternating layers or silicon oxide and silicon nitride or combinations thereof (col. 4, lines 42-45).

16. With respect to claim 7, Baw-Ching Perng et al. also shows the method as claimed as: the sidewall spacer is formed using a blanket deposition process and a dry etch process (col. 4, lines 56-60, dry etch refer to RIE in the reference).

17. With respect to claim 8, Baw-Ching Perng et al. also shows the method as claimed as: the at least one first doped region is formed using an ion implantation process and an annealing process (col. 3, lines 43-45).

18. With respect to claim 10, Baw-Ching Perng et al. also shows the method as claimed as: a method of forming an integrated circuit transistor, comprising: proving a semiconductor substrate with gate structure formed thereon (Fig. 1, 1, 3); blanket

deposition at least one first dielectric layer (5) overlying the semiconductor substrate without performing an etch process on the at least one first dielectric layer (Fig. 2), wherein the at least one first dielectric layer comprises at least one first portion along at least one sidewall of the gate structure; wherein the at least one first dielectric layer comprises at least one second portion outside the gate structure along the surface of the semiconductor substrate (Fig. 3); performing a first ion implantation process to form at least one first doped region (4) in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer, wherein the at least one second portion of the at least one dielectric layer remains overlying the at least one first doped region.

19. With respect to claim 12, Baw-Ching Perng et al. also shows the method as claimed as: a thickness of the at least one first dielectric layer ranges from about 10 angstroms to about 350 Angstroms (Col. 3, lines 51-53).

20. With respect to claim 13, Baw-Ching Perng et al. also shows the method as claimed as: the at least one first dielectric layer is silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride or combinations thereof (col. 3, lines 51-53).

21. With respect to claim 14, Baw-Ching Perng et al. also shows the method as claimed as: depositing at least one second dielectric layer overlying the at least one first dielectric layer (Fig. 2, 6a), etching the at least one second dielectric layer to form at least one sidewall spacer along the at least one sidewall of the gate structure (Fig. 3, 6b); and performing a second ion implantation process to form at least one second

doped region (7) in the semiconductor substrate laterally adjacent to the at least one sidewall spacer.

22. With respect to claim 15, Baw-Ching Perng et al. also shows the method as claimed as: the at least one second dielectric layer is silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof (6b, col. 4, lines 42-45).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 5, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baw-Ching Perng et al. (6,498,067 dated 12/24/2002) in view of Schuegraf et al. (6,140,203 dated 10/31/2000,) and Samavedam et al. (6423632 dated 07/23/2002).

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baw-Ching Perng et al. (6,498,067 dated 12/24/2002) in view of Samavedam et al. (6423632 dated 07/23/2002).

3. With respect to claim 5, Baw-Ching Perng et al. shows the process as claimed and as described in the preceding paragraphs, but fails to expressly disclose the formation of the at least one dielectric layer is a blanket deposition by a chemical vapor deposition (CVD) process using tetraethylorthosilicate.

4. With respect to claim 5, Samavedam et al. teaches at least one dielectric layer (52) is a blanket deposition by chemical vapor deposition (CVD) process using tetraethylorthosilicate (TEOS) (col.4, lines 20-25). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dielectric layer as shown by Samavedam et al. because TEOS can be use to isolation of gate in the semiconductor transistors.

5. With respect to claims 9 and 11, Baw-Ching Perng et al. shows the process as claimed and as described in the preceding paragraphs, but fails to expressly disclose the at least one dielectric layer becomes a densified material which exhibits an etch rate less than about 200 Angstroms/minute in a 100:1 HF solution.

6. With respect to claim 9 and 11, Schuegraf et al. teaches at least one dielectric layer (48) becomes a densified material, which exhibits rate less than about 200 Angstroms/minute in a 100:1 HF solution (48, col. 3, lines 40-45). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dense dielectric layer as shown by Schuegraf et al. in the

claimed range because TEOS density can be also characterized relative to an etch rate of about 175 Angstroms/minute. Over lapping ranges establish a prima facie case of obviousness. In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 514 F.2D 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Ullah whose telephone number is 571-272-1415. The examiner can normally be reached on 8-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MICHAEL LEBENTRITT can be reached on (571)272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EMU

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SUPERVISORY PATENT EXAMINER